METHOD OF MANUFACTURE OF PROGRAMMABLE CONDUCTOR MEMORY

Abstract of the Disclosure

Programmable conductor memory cells in a stud configuration are fabricated in an integrated circuit by blanket deposition of layers. The layers include a bottom electrode in contact with a conductive region in a semiconductor substrate, a glass electrolyte layer that forms the body of the cell and a top electrode layer. Under the influence of an applied voltage, conductive paths grow through or along the cell body. The layers are patterned and etched to define separate pillars or cells of these stacked materials. A liner layer of an insulating material is deposited over the cells and acts as a barrier to prevent diffusion of the metal in the cell body into other parts of the integrated circuit. Remaining regions between the cells are filled with an insulating layer. At least some of the insulating layer and some of the liner layer are removed to make contact to the top electrode layer of the cell and to the substrate.